Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399

March 25, 2022

Sreenivas Ramaswamy
Senior Policy Advisor, Office of Policy and Strategic Planning
U.S. Department of Commerce
1401 Constitution Ave NW
Washington, DC 20230

RE: Microsoft Comments Responding to U.S. Department of Commerce *Request for Public Comments on Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry*

Dear Mr. Ramaswamy:

Microsoft appreciates the opportunity to respond to the U.S. Department of Commerce's (Commerce) request for public comments entitled *Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry (the RFC)*. As Commerce and the National Institute of Standards and Technology (NIST) demonstrate their collective leadership in developing a national strategy for the future of the U.S. semiconductor industry, Microsoft offers the comments and recommendations below, followed by specific responses to the RFC's four areas of inquiry. We welcome the opportunity to continue the conversation on how to support these important issues beyond these comments.

I. General Recommendations

Microsoft appreciates Commerce's commitment to realizing the promise of the *Creating Helpful Incentives to Produce Semiconductors* (CHIPS Act) and welcomes the Biden-Harris Administration's support of $52B in funding for the CHIPS Act.[1] Prioritization of funding for leading edge facilities and the equipment to enable the development and production of leading-edge technology will support the continued innovation of technology – from devices, to gaming, to cloud solutions – that leads to domestic economic growth and will enable National Security and Defense technologies to continue to process information at the highest performance levels.

Semiconductors are essential to virtually all sectors of the economy and are the building blocks of critical and emerging technology. While the U.S has historically dominated many parts of the semiconductor supply chain, U.S. leadership position has—as recognized by this RFC—faced numerous challenges over the last several years. Further, as highlighted by business leaders representing major companies in their letter to Congressional leaders on December 1, 2021[2], demand for these critical components has outstripped supply, creating a global chip shortage resulting in consumer frustration, and lost growth and jobs in the economy. The shortage has been further exacerbated by Russia's war with Ukraine, which has strained the supply chain for critical minerals and other raw materials and exposed further vulnerabilities in the semiconductor supply chain. All of this taken together reinforces the need for

[1] FACT SHEET: Biden-Harris Administration Bringing Semiconductor Manufacturing Back to America | The White House)
[2] Microsoft Word - CEO letter on CHIPS and FABS.docx (semiconductors.org)

increased investment in research, design, and manufacturing capacity both domestically and by allied nations.

For the U.S. to maintain its technology leadership, we must make investments to promote a strong, skilled advanced manufacturing workforce. We should also strengthen and diversify the semiconductor supply chain by building out U.S. manufacturing capacity and partner with allied nations towards the same objective. American innovation should lead to American growth. However, for the complex semiconductor industry, effectively translating innovation into domestic growth requires strategic and targeted investment – and the need for investments is more urgent than ever. Existing semiconductor technology is rapidly approaching the physical limits of two-dimensional scaling underpinning Moore's law[3] and many emerging and advanced technologies rely on a secure supply of chips – from 5G, Internet of Things (IoT), Artificial Intelligence (AI), data centers and cloud computing, to quantum computing, and supercomputer development.

Microsoft has identified numerous challenges facing the semiconductor supply chain in its discussions with industry and government and in prior filings advancing the dialogue opened by the Administration with Executive Order 14017, America's Supply Chains[4]. For example, we submitted comments on November 8, 2021, in response to the Department of Commerce's Request for Public Comments on Risks in the Semiconductor Supply Chain, 86 FR 53031[5] and in response to the Department of Energy's Notice of Request for Information on Energy Sector Supply Chain[6]. As noted in those comments, an array of obstacles, including long lead times, infrastructure constraints, and cost competitiveness, hinder the U.S. government's ability to address semiconductor supply chain challenges.

To address these challenges requires more than investment in the U.S. as contemplated by this RFC, but also engagement by allied nations working together to build a supply chain coalition that will be able to withstand geopolitical disruptions and ensure continuity and security in the face of future disruptions. Enhanced multilateral cooperation on supply chain resiliency and security efforts in a way that's consistent with global partnerships is also critical to address these challenges. Initiatives proposed by the European Commission under the umbrella of the European Chips Act, the U.S.-EU Trade and Technology Council, and the evolving Indo-Pacific Trade strategy, each represent a unique opportunity to strengthen and diversify supply chains and to build complementary and diverse manufacturing and research capabilities across allied-nations.

To protect U.S. semiconductor leadership, manufacturing continually fueled by world-leading research and development is key. The programs envisioned by the *2021 National Defense Authorization Act* – the National Semiconductor and Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP) – are essential to enable the planning and design of the necessary programs to incentivize investment for semiconductor manufacturing facilities and associated ecosystems, and to create a shared infrastructure to accelerate semiconductor research related to advanced metrology. These programs will lay the groundwork for the innovation infrastructure needed for the U.S. to ensure a robust domestic semiconductor industry, resilient supply chains, and sufficient

---

[3] *American Innovation, American Growth: A Vision for the National Semiconductor Technology Center*, Mitre Engenuity, November 2021 ("Mitre Report"

[4] Federal Register: America's Supply Chains

[5] https://www.regulations.gov/comment/BIS-2021-0091

[6] Regulations.gov (Comment ID: DOE_HQ-2021-0020-0088: Semiconductors - Cybersecurity - Microsoft Comments - DOE RFI Energy Sector Supply Chain 1-15-2022)

chip supply to power the U.S. economy and given their integrated nature, would benefit from being combined into a single program.

With a foundational charter focused on research and prototyping of advanced semiconductor technology, the NSTC is, as recognized in the recent white paper from Mitre Engenuity, a unique opportunity to strengthen the United States's ability to translate innovation into "manufacturable, market ready technology domestically" to overcome the manufacturing "valley of death" that results in promising research failing due to inadequate funding and resources.[7] While the United States excels at research and development, it has struggled to transition breakthroughs into scaled production.

The plan and future for the NSTC should be defined by programs that push the envelope of the possible with science and technology. The NSTC should be empowered to prioritize and pick these breakthrough challenges that lead to truly revolutionary science and technology. The NSTC is envisioned as a public-private partnership to conduct research, development and prototyping of advanced semiconductors, support startups and small businesses, and provide workforce training programs. The NSTC governance board should plan to define these breakthrough challenges and serve as a centralizing hub, convening and bringing people together in public-private partnerships with industry, academia, and government to marshal semiconductor expertise and resources to deliver breakthroughs in chip innovation and production across the valley of death. To achieve these goals, and to enable industry to innovate and prototype to scale, the NSTC should establish a governance model that affords all participants access to the output of any consortia, including defining a clear and equitable framework for use of intellectual property.

As stated above, breakthrough challenges are revolutionary products and services that are typically full stack problems requiring knowledge of materials, circuits, architecture, operating systems and applications. Facilitating and executing these breakthrough challenges will be key. Choosing and running the breakthrough challenges must be a central part of the NSTC. Once a breakthrough challenge is launched, the NSTC should seek participation from all the entities – corporations, academia, government, and startups – that have technology and science that accrues to the success of the breakthrough challenge. Finally, the NSTC should be empowered to inform and drive changes associated with workforce development. We simply need more **inspired and educated** STEM people -to meet the demands of today's industry and to unlock the breakthrough challenges of the future.

To achieve these goals, as discussed in greater detail below, an integral part of the technology network must be an academic component that will have the dual mission of education and advancing the R&D technology pipeline into the NSTC and NAPMP agenda. This is necessary to strengthen the "lab-to-fab" pathway which will accelerate the transition of viable technologies with a 5-10-year horizon to development and high-volume manufacturing—driving U.S. innovation and differentiation in chip manufacturing, packaging, and testing. The work with academia should be designed to access talent from the broadest range of institutions across the nation including Historically Black Colleges and Universities (HBCUs), other minority-serving institutions (MSIs), 4-year colleges, community colleges, and integrated high school to college programs (e.g., P-TECH).

The Importance of Cybersecurity for the Semiconductor Supply Chain

Security of our digital economy is core to U.S. national prosperity, and the last two years have highlighted not only challenges with supply chain logistics, but also supply chain cybersecurity.

[7] Mitre Report, p. 4

Commerce has traditionally played a central role in enhancing the security of our cyber posture through developing and maintaining the NIST Cybersecurity Framework (CSF), Special Publication (SP) 800-161 (*Cybersecurity Supply Chain Risk Management Practices for Systems and Organizations*), and other related standards efforts. And Commerce has played a key role in developing and implementing the recent Executive Order on Improving the Nation's Cybersecurity (EO 14028) that will make our software supply chain more robust against attack.

With its recently announced public-private partnership on Improving Cybersecurity in Supply Chains, Commerce is taking the important step of applying lessons learned in the software and operational risk management context to technology supply chains more broadly, including for hardware. As Commerce continues its leadership role in developing a national strategy, we firmly believe it is an ideal time to extend its role in cybersecurity to meet this critical need.

Microsoft's overall vision for securing the silicon and microelectronics supply chain is three-fold:

- *Continuity*. Ensure that bottlenecks in the supply chain have limited exposure to disruptions caused by geopolitical, natural disaster, or other location-specific risks.
- *Transparency and efficiency*. Enable companies and government agencies to predict, avert, and mitigate supply disruption due to inefficiencies, misallocation, or other unexpected events that can cause economic harm.
- *Security*. Protect U.S. companies' IP and U.S. citizens' data as data and components circumnavigate the globe. Ensure proper functionality of systems required for the U.S. Government, critical infrastructure, and products that are critical for life and safety.

There are many individual processes in the industry today that enhance the security posture for hardware systems. However, there is no single accepted standard or agreement to prohibit the supply chain as a cyberattack vector, and no system or standard that enables traceability or visibility of compliance. For example, when an end user purchases a commercial computing system today, they may be able to periodically investigate the security practices of the vendor, but there is no real-time validation for a given shipment, and they will quickly lose visibility into the complex chain of custody, and the security practices of component suppliers. In effect, there is no audit trail, and individual companies are not able to solve this problem alone.

This is exactly the problem that EO 14028 is addressing for software, and we are encouraged that, through the recently announced public-private partnership for Improving Cybersecurity in Supply Chains, Commerce is extending its learnings and aiming to play a critical role in supporting a similar solution for hardware. As that effort gets underway, we recognize that there are many directions in which it might appropriately grow given the breadth of the challenge and opportunity. To strike the right balance, an example can be seen in Section 224 of the Fiscal Year 2020 National Defense Authorization Act, which mandated a framework for microelectronics security and standards; this framework could be used by Commerce to include similar compliance requirements in foundry investment agreements. A related vector that extends to the development of prototypes is the Rapid Assured Microelectronics Protypes (RAMP) program, that has spurred innovation and engagement. This program is emblematic of the complexity of the industry, since demonstrating a prototype in two different foundries required a team of Microsoft plus 14 subcontractors. The RAMP program nonetheless demonstrates the power of the government in creating communities that would otherwise have been nearly impossible to gather. We also encourage Commerce to consider how to build upon industry-led efforts, such as the IETF Supply Chain Integrity, Transparency, and Trust (SCITT) project (Supply Chain Integrity, Transparency,

and Trust · GitHub) that aims to enable the secure automated exchange of verifiable artifacts for all types of technology, including software and hardware, between all participants in a supply chain.

While Microsoft is committed to continual improvement in cybersecurity, we believe there is a high risk that such a broad endeavor for hardware security would not succeed without the support of Commerce. Commerce engagement and leadership through NIST's new public-private partnership effort has the potential to provide a strong tailwind for success. Additionally, secure silicon regardless of manufacturing location should be a priority, and Microsoft has solutions that could be prototyped at the NSTC. We look forward to deeper discussions and demonstrations on how we can partner to address this critical need.

The Importance of Cryptographic Agility and Post-Quantum Cryptography in Semiconductors

An important consideration for future silicon architectures is the degree to which they support cryptography-related requirements and use cases, in particular the design principle of *cryptographic agility* and secure and performant implementation of *post-quantum cryptographic (PQC) algorithms.* Cryptographic agility is a security design principle that allows computing systems to be easily reconfigured from using one cryptographic algorithm to another. This property is extremely important when designing secure systems to be robust against cryptographic attack or cryptanalytic weaknesses in underlying algorithms. Cryptographic algorithms can weaken and fail over time due to improvements in cryptanalytic techniques; when that happens, devices need to be reconfigured quickly to no longer use or depend upon the now-weakened algorithms.

Our ability to transition devices and ecosystems to new cryptographic algorithms is already being tested by the upcoming transition to post-quantum (a.k.a. quantum-resistant) public-key cryptographic algorithms[8] [9]. NIST is currently in the process of selecting new public-key algorithms that are designed to be secure even against an adversary with access to an industrial-scale quantum computer (>= 1,000,000 physical qubits). New semiconductor architectures should consider functional elements designed for these new PQC algorithms; many of the candidate PQC algorithms will benefit from larger multiplier units and more parallel multiplier units on the die. Specialized instructions designed to accelerate standard cryptographic hash functions like SHA-3 would also be helpful to the cryptographic community and its customers.

In addition to potentially providing functional units designed to improve the runtime and side-channel security of widely deployed cryptographic algorithms, new architectures and manufacturing processes would also benefit by including security and cryptography features aimed at ensuring the integrity of the semiconductor manufacturing process and supply chain.

II. Specific Recommendations

Semiconductor Financial Assistance Program Questions 1, 2, 3, 7, 8 & 10

[8] Brian LaMacchia, "The Long Road Ahead to Transition to Post-Quantum Cryptography," *Communications of the ACM*, January 2022, Vol. 65 No. 1, Pages 28-30

[9] Campagna M., LaMacchia B., & Ott D. (2020) *Post Quantum Cryptography: Readiness Challenges and the Approaching Storm*. https://cra.org/ccc/resources/ccc-led-whitepapers/#2020-quadrennial-pape

Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399

Question 1: The term ''semiconductor'' is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of ''semiconductor'' for purposes of a semiconductor manufacturing incentives program?

Microsoft recommends applying a definition for "semiconductor" sufficiently tailored to target technologies beyond silicon. The definition should promote core strategic products, including advanced logic, discrete/analog/optoelectronics (DAO), and memory devices that primarily rely on silicon, silicon-germanium, and essential compounds such as Gallium arsenide (gaAs), and gallium nitride (GaN) as the active materials.

Question 2: Section 9902 permits a ''consortium'' of public and private entities to apply for funding. What factors would public and private entities consider determining whether to apply for funding as part of consortium? How would private entities determine whether to work with a public entity as part of a consortium? How would a private entity consider working with other private entities (such as customers, equipment manufacturers, or capital providers) as part of a consortium?

The NSTC should establish a governance model that affords all participants access to the output of any consortia, including establishing an IP framework that ensures contributors can freely use that intellectual property.

Question 3: Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?

We recommend prioritizing leading-edge facilities and equipment as the center of any long-term strategy to enable the development, production, and onshoring of leading-edge technology referenced in response A.1. This prioritization will support the continued innovation of technology – from devices, to gaming, to cloud solutions – and lead to domestic economic growth. This prioritization will also enable National Security and Defense technologies to continue to process information at the highest performance levels.

In parallel to enabling this long-term strategy, we also support the inclusion of $2B in the CHIPS Act for legacy technology funding, and recommend criteria that apply an ecosystem-wide view that considers total aggregate demand to ensure adequate supplies of legacy technologies remain available where leading edge technologies are neither cost effective nor required for the application.

Question 7: How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?

To encourage additional and new private capital, it will be important to enable and demonstrate a return on the investment. This could be a specific component or product that is being developed, or part of a licensing revenue stream for IP. It could be other ideas where capital can get a significant return on investment. Private capital should have opportunities to invest in the program but will need a compelling reason to participate.

Question 8: How can Federal funds incentivize the creation of a broad semiconductor ecosystem that includes producers of semiconductor manufacturing equipment and other upstream suppliers? What are the largest supply imbalances with respect to manufacturing equipment, tools, materials, and chemicals that need to be addressed by U.S. investment?

Federal funds should incentivize the onshoring and establishment of domestic facilities capable of supporting leading edge manufacturing facilities and incentivize workforce development programs, while also ensuring an adequate supply of legacy technology remains available as discussed in Question 3 above.

Question 10: Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?

Voluntary breakthrough challenges that encourage large entities to partner with medium and small business suppliers will be beneficial if the objectives of the collaborating partners are aligned. Partnership mandates should be discouraged and would likely have a negative impact on participation and investment.

National Semiconductor Technology Center Questions 1 and 4 & Advanced Packaging Manufacturing Program – Generally

The work of the NSTC and the National Advanced Packaging Manufacturing Program (NAPMP) should be deeply integrated and the two programs could be combined. Microsoft supports the general framework for the NTSC outlined in the report released by *ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA: Bringing the Best Research and Development to The National Semiconductor Technology Center*[10]. It offers a vision for an innovation ecosystem, with *geographically disbursed regional hubs* and centers of excellence, as the main technical driver of the NSTC and NAPMP. This technology network would work with the Departments of Commerce, Defense, and Energy in support of the agenda laid out in the FY 2021 NDAA, including related programs such as metrology R&D at NIST, the roadmap to support research and university collaborations, and direct development, prototyping and manufacturing investments that would scale commercially to ensure the goals of the NSTC and NAPMP are met.

As envisioned, this center for technology innovation would establish a pathway for this urgent investment. It would uniquely accelerate the U.S. transformation into a secure semiconductor powerhouse. To maintain leadership, America's semiconductor industry will need to be continually refreshed by world-leading research and development, as the FY 2021 NDAA recognizes. That research and development is the focus of this vision. At its baseline, the governance model should establish that all relevant parties are afforded equivalent access to the resulting collaborations, including the ability to leverage the IP - all need to have equivalent access. NSTC must also establish clear parameters on the use of IP to ensure contributors are afforded free and clear access to the research, design, and proof of concept collaborations.

The technology network would be responsible for creating, coordinating and executing on a strong technical agenda that accelerates and enables the wider goal of the FY 2021 NDAA– U.S. semiconductor

[10] NSTC R&D - Vision Document - V6 (ny.gov) (February 2022)

and advanced packaging leadership. This can be accomplished through proven chip innovation results, expansive partnerships, leveraging state-of-the-art facilities and transfer-to-manufacturing expertise.

Question 1: Based on the functions outlined in section 9906(c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap between R&D and commercialization. What attributes are most important for the NSTC to possess or provide to the community (e.g., ease of access, a broad suite of leading edge tools managed as central facility, a collaborative research environment)? What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?

The NSTC must be empowered to not only identify, resource, and execute Breakthrough Challenges, but also to follow the investment through implementation to measure performance. To enable this end-to-end insight, the NSTC advisory board should be comprised of innovative and experienced technology product experts with the technological insights to create the necessary processes to deliver on selection, resourcing, and execution. This must all be done with a governance model that promotes neutrality and excellence. Additionally, it is critical for the NSTC to have the functional capability to prototype full stack solutions to overcome the manufacturing "valley of death" that has bedeviled investments, as well as support the process to scale to full production.

Question 4: How should the NSTC connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

CHIPS funds a DoD-led research initiative which is a network of research hubs, but focused on academia called "The Commons". It is critical for Commerce and DoD to be aligned and make the NSTC and CHIPS complementary. While some overlap is inevitable, university facilities should complement the NSTC. It is also critical that the governance for the Commons and other research programs be led from a research/academic perspective and informed by an industry advisory board whereas the NSTC governance should be led by industry and informed by an academic/research advisory board. In other words, the guiding governance principle should be for these complementary programs to commonality on their respective advisory boards so that Commons research funnels into the NSTC. For this to be effective, the NSTC needs visibility into what is in development, and the Commons needs to understand practical challenges in scaling.

We envision the National Microelectronics Commons as complementary to the NSTC, and as a network of staffed facilities designed to make the lab-to-fab transition for semiconductor technologies. The Commons would provide *flexibility at scale*—the materials and process flexibility of a university lab at the scale of an industry production fabrication facility—and thus form a bridge between today's isolated innovations and the integrated systems that will enable tomorrow's communications systems, artificial intelligence, internet-of-things, robotics, smart electricity grid, and cognitive computing. The Commons should be led first from research and academic perspectives and informed by an industry advisory board. As a public-private partnership, the Commons would serve *all* American users—from universities, start-ups, and corporations—with a sliding-scale, fee-for-use model to access equipment and staff time.

The Commons campuses could also include leasable private space to build critical masses of American semiconductor research, prototyping, and manufacturing.

Semiconductor Financial Assistance Program Questions 11 and 12 & Semiconductor Workforce Question 1

Question 11. Section 9902 requires a covered entity to make commitments to invest in workers and communities, including through training and education benefits and programs to expand employment opportunity for economically disadvantaged individuals. What constitutes a baseline commitment to worker training in the semiconductor industry and what other workforce investments should be considered? Are there international best practices or cooperation upon which your company finds beneficial? What other community investments should be considered beyond worker training and employment opportunities? How can worker training, other workforce commitments, and other community commitments be maximized and how should program participants be held accountable to their commitments? What types of programs exist, or could be expanded, to improve access for economically disadvantaged individuals to these workforce and community commitments and opportunities?

Worker training should be a key component of any programs supported by incentives to Covered Entities. In order to support increased production and innovation in the United States, the semiconductor industry will need a significant number of skilled workers across the educational and training spectrum. This includes individuals skilled in technical manufacturing and production occupations—encompassing factory technicians and line workers—as well as electronics and electrical engineers and chip designers. A number of positions in the industry can be fulfilled through community college Associates degrees or equivalent training, particularly in production operations.

Since the goal of the underlying legislation is to not only expand the skilled workforce but to also reach a broader set of communities and individuals with these employment opportunities. It is critical that Covered Entities partner with a diverse range of institutions, including the public workforce system, community colleges, technical colleges, four-year institutions including HBCUs and MSIs, and non-profit intermediaries that can help reach underserved communities, identify talent, and provide support to help students and workers succeed. Covered Entities should be required to demonstrate that they are partnering with these organizations to provide job training and education, and to support individuals to complete that training and gain exposure to roles in the industry. Finally, such partnerships should entail opportunities for hands on learning and chances to learn about the specific roles available in the semiconductor industry. Engagement should include learn-and-earn strategies, such as apprenticeships, paid internships, work-study, and paid research opportunities, as well as job fairs, shadowing, and mentorship events. Covered Entities should work with third-party stakeholders to ensure that STEM education and training requirements are up to date. Such partnerships should also ensure that training programs can take advantage of current technology and help students and workers attain skills that are immediately useful for in-demand roles. These contributions should incorporate financial support as well as in-kind support, through the provision of technology or participation by employees in training and mentorship programs. Scholarships and hands-on opportunities to help individuals from groups underrepresented in the industry complete degrees in necessary fields and learn about the industry could also be a key component of Covered Entities contributions.

Covered Entities should also demonstrate, as appropriate, how they are incorporating strategies to upskill their existing workforce and providing opportunities for individuals to stay current with trends in the industry and where possible to move into more skilled roles.

Finally, data about effective training and upskilling interventions is sparse. Recipients of these funds should be required to report back on the types of training and programs they have engaged in (internal training, supporting workers to pursue external training or skills, scholarships for attaining post-college degrees or coursework, etc.) and the outcomes.

Question 12. Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?

The United States continues to be challenged in generating enough K-12 graduates who are interested in STEM and sufficient students majoring in technical fields at the college level. Some key steps the federal government can take to support expanded technical education include additional appropriations for computer science teaching at the K-12 level. Covered Entities could also contribute to K-12 technology education through models such as Project Lead the Way and Microsoft's TEALS (Technology Education and Literacy in Schools) Program.

While the increased emphasis on K-12 computer science enrollment is a necessary condition to expand the talent pipeline for the semiconductor industry more broadly, it is not sufficient to achieve the expansion that is sorely needed. We have a deficit of individuals with the skills needed for semiconductor industry engineering and production—such as materials science, electrical engineering, and physics and need individuals to receive training for all levels of semiconductor positions – including material scientists, chip designers, chip testers, architects, and manufacturing engineers. The federal government should consider how to create more scholarships or other financial incentives for individuals to pursue these majors or for computer science students to gain exposure and experience with roles in the semiconductor field.

In other countries technical apprenticeships that have strong engagement from industry have made a significant contribution to expanding these pipelines—the federal government could consider how grants or other incentives can help to galvanize private sector coordination to establish industry sector programs. Finally, Covered Entities should participate in federal agency information collection and work with private sector data sources to ensure that real-time data about industry needs is being shared with policymakers and with educational institutions.

Question 1: What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399

To support increased production and innovation in the United States, the semiconductor industry will need a significant number of skilled workers across the educational and training spectrum. This includes individuals skilled in technical manufacturing and production occupations, encompassing factory technicians and line workers; developers and designers, including electrical engineers, circuit designers, materials scientists, circuit designers, architects, device developers; and individuals needed to work on full stack solutions to bring disparate disciplines together into a breakthrough challenge.

We are facing shortages at every point in the talent pipeline in the United States and the consequence is that the United States will lose our leadership in building devices that are critical to everyday functioning—phones, consoles, datacenters—as well as products that are vital for our national security.

III. Conclusion

We appreciate the opportunity to provide Commerce feedback to inform its important work to incentivize the domestic semiconductor ecosystem. We encourage Commerce and other administration stakeholders to continue engaging actively with the private sector and others to identify actionable solutions to strengthen the U.S. semiconductor leadership. We look forward to continuing to partner with U.S. Government and if you have additional questions or would like to discuss the comments further, please contact me at Sarah.ONeal@microsoft.com or (202) 365-9011.